# Tutorials #4

## Exercise 01:

We have a laptop equipped with a quad-core processor with a frequency of 1.4 GHz and three cache memories, L1 with a size of 256KB, L2 with a size of 1MB and L3 with a size of 12MB. The hit rate in L1 is 80%, while the hit rate in L2 is 90%. The mis rate in L3 is 10%. The processor requires 3 cycles to load an instruction into L2, 2 cycles to load an instruction into L1 and 5 cycles to load an instruction in L3.

- 1. Calculate the number of blocks in L1, L2 and L3, knowing that the size of an L1 block is 128B.
- 2. Calculate the time required for the execution of a program with 10<sup>6</sup> instructions, considering that an instruction takes 10 cycles to execute.

### Exercise 02:

A desktop computer is equipped with a sixth-generation i7 processor with a 2-core configuration. The processor operates with an internal clock of 2.4 GHz and has four super scalars. The first super scalar contains 8 units and processes complex instructions with an average time of 2 cycles per unit. The second one contains 6 units designed for multimedia instructions with an average time of 2 cycles per unit. The third super scalar contains 5 units specialized in arithmetic and logic instructions with an average processing time of 1 cycle per unit and the last one contains 5 units specialized in flotant instructions with an average processing time of 2 cycle per unit.

- 1. Calculate the MIPS.
- 2. Calculate the average execution time of a program with 10<sup>9</sup> instructions composed of 25% arithmetic and logic instructions, 25% of flotant instructions, 35% multimedia instructions, and 15% complex instructions.

### Exercise 03:

The computers in the machine room have an identical configuration, featuring a dual-core processor with a clock speed of 2.1 GHz and a 32-bit MATSONIC motherboard with a 1600MHz front-side bus (FSB). The processor is equipped with pipeline technology with 6 stages and 3 cycles for each stage.

- 1. Calculate the computer's bandwidth.
- 2. Calculate the time required for the execution of a program with 10<sup>6</sup> instructions.

#### Exercise 04:

We want to execute a program with 10<sup>9</sup> instructions on a computer containing an Intel i5 processor with a 4-core configuration and a frequency of 3 GHz. The processor is installed on a motherboard with a 2433MHz FSB and a maximum RAM capacity of 16GB. The processor is equipped with pipeline and super-scalar technology. It also has two cache memories, L1 with 128 blocks and L2 with 16 blocks. The first super scalar contains 7 units, and it requires 1 cycle per unit. The second super scalar contains 6 units and consumes 2 cycles per unit.

- 1. Calculate the MIPS.
- 2. Calculate the maximum number of executions in parallel.
- 3. Calculate the size of L1, knowing that the size of L2 is 16MB.
- 4. Calculate the average execution time of the program, given that the cache miss rate is 40% in L1 and 20% in L2, and the processor needs 5 cycles to load an instruction into L2 and 3 cycles to load an instruction into L1.